

7
Cordell
A2
(b) forming an electrically insulating layer having a[n] pair of opposed outer faces, one of said outer faces disposed on said surface one of said substrate or said device wafer, said electrically insulating layer having an electrical interconnect structure disposed therewithin, a portion of said interconnect structure extending substantially to said one of said outer faces of said electrically insulating structure; and

(c) then bonding the other of said outer [surface] faces of said electrically insulating layer to the said surface of the other of said substrate or device wafer.

Amend claim 2 as follows:

2. (Amended) The method of claim 1 [2 wherein a portion of said electrically insulating layer is disposed between said interconnect structure and at least one of said substrate or device wafer,] further including the step of applying a voltage across [said] a portion of said electrically insulating layer sufficient to break down said portion of said electrically insulating layer while maintaining the integrity of the remainder of said SOI structure

Amend claim 7 as follows:

13
Sub 7
B2
7. (Amended) A method of forming an SOI structure, comprising the steps of:
providing [having] a device layer having at least one of active or passive elements on a surface thereof, a substrate having at least one of active or passive elements on a surface thereof and an electrically insulating layer having an interconnect structure disposed therein and extending to a surface thereof, said interconnect structure separating a portion of said device layer from said substrate; [comprising the steps of:]

[(a)] forming a substantially planar surface comprising areas of one of said device layer and said substrate and areas of said electrically insulating layer; and

Cancel 13

[[b)] then bonding said surface to the other of said substrate wafer and device layer.

Amend claim 8 as follows: 9

8. (Amended) The method of claim [8] 7 further including the step of forming an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting at least one of said device layer and said substrate.

Cancel claims 10 and 11 without prejudice.

Amend claim 18 as follows:

14 18. (Amended) A method of fabricating an integrated circuit which comprises the steps of:

(a) providing a device layer having at least one of active or passive elements on a surface thereof;

(b) providing a substrate having at least one of active or passive elements on a surface thereof [spaced from said device layer];

(c) providing [bonding] a [buried] dielectric bonded to one of said device layer and said substrate having an interconnect disposed therein and extending to at least one surface thereof;

(d) then bonding said dielectric [therein] to [one] the other of said device layer and said substrate to form an interface with said one of said device layer and said substrate[;] and [(d)] forming an electrically conductive path across said interface to said interconnect [directly beneath said device layer].